



# SIM8200G

## Pin Definitions

5G Module

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## Version History

Date	Version	Description of change	Author
2019-07-09	V1.00	Initial release	ChangshunTan
2019-07-19	V1.01	1、 UpdatePIN Assignment 2、 Update PIN Description 3、 Update GPIO Alternate function 4、 Delete Antenna reference design	ChangshunTan
2020-03-17	V1.02	Update document template	Zhiqiang Liu

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# 1. Hardware Block Diagram

The block diagram of SIM8200G is shown in the following figure.

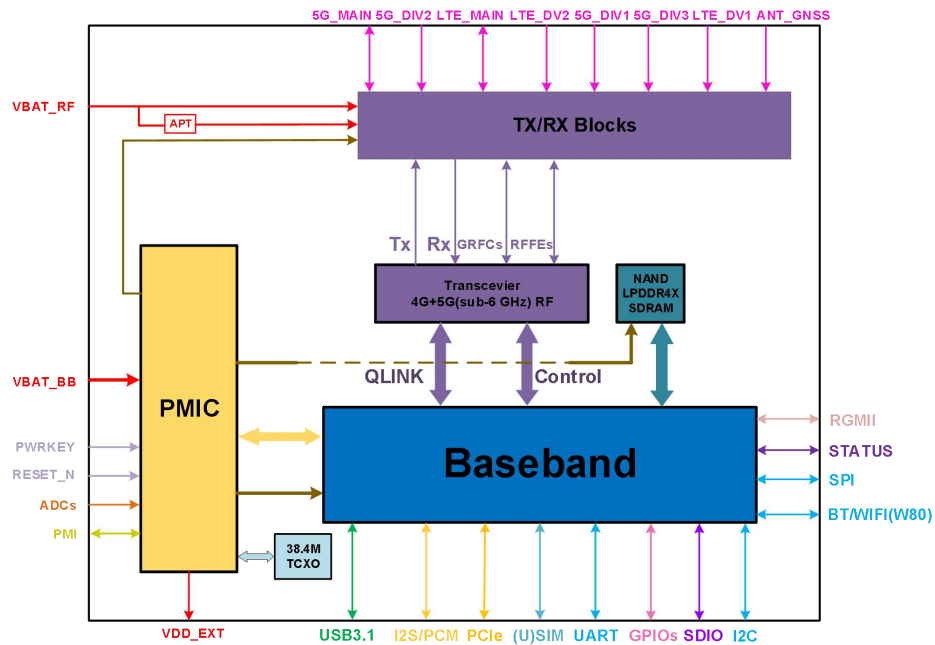


Figure 1: SIM8200G module block diagram

## 2. Package Information

### 2.1 Pin Assignment Overview

The SIM8200G module has 369 LGA pins. Customer design should match pins functions. The following figure is the pin assignment of the module.

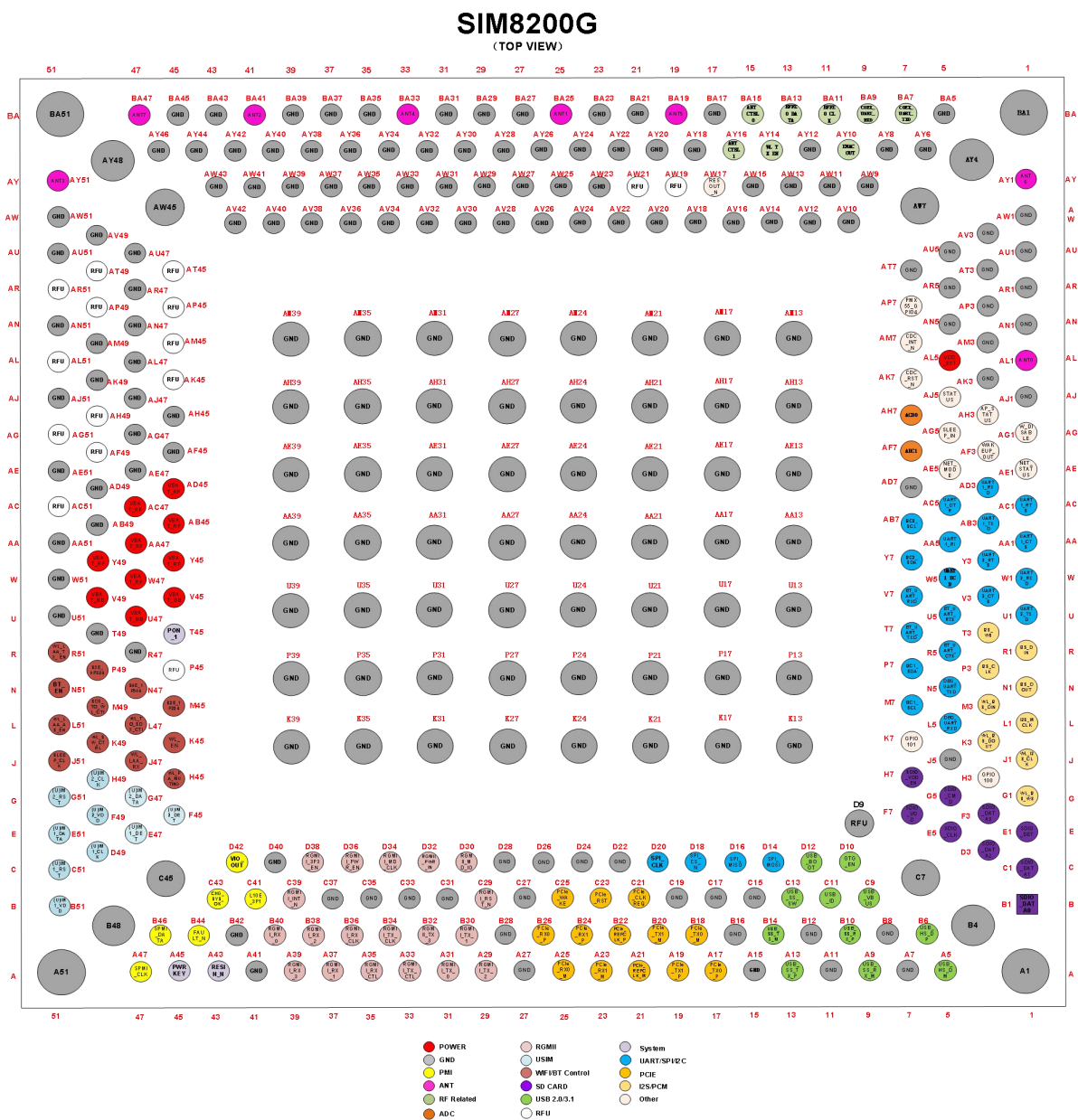


Figure 2: Pin assignment



## 2.2 PIN Description

**Table 1: IO parameters definition**

Pin Type	Description
PI	Power input
PO	Power output
AI	Analog input
AIO	Analog input /output
DIO	Bidirectional digital input /output
DI	Digital input
DO	Digital output
PU	Pull up
PD	Pull down

**Table 2: DC parameters definition**

Voltage domain	Parameter		Min	Typ	Max
P2	VDD_P2=1.8V				
	VOH	High level output	1.4V	-	-
	VOL	Low level output	0V	-	0.45V
	VIH	High level input	1.27V	-	2V
	VIL	Low level input	0V	-	0.58V
	Rp	Pull up/down resistor	10K ohm	-	100K ohm
	VDD_P2=3.0V				
	VOH	High level output	2.25V	-	3.0V
	VOL	Low level output	0V	-	0.375V
	VIH	High level input	1.84V	-	3.25V
	VIL	Low level input	0V	-	0.75V
	Rp	Pull up/down resistor	10K ohm	-	100K ohm
P3	VDD_P3=1.8V				
	VOH	High level output	1.35V	-	1.8V
	VOL	Low level output	0V	-	0.45V
	VIH	High level input	1.26V	-	2.1V
	VIL	Low level input	0V	-	0.6V
	Rp	Pull up/down resistor	20K ohm	-	60K ohm
P4	VDD_P4/P5=1.8V				
	VOH	High level output	1.44V	-	1.8V

	VOL	Low level output	0V	-	0.4V
	VIH	High level input	1.26V	-	2.1V
	VIL	Low level input	0V	-	0.36V
	Rp	Pull up/down resistor	10K ohm	-	100K ohm
	VDD_P4/P5=3.0V				
	VOH	High level output	2.4V	-	3.0V
	VOL	Low level output	0V	-	0.4V
	VIH	High level input	2.1V	-	3.05V
	VIL	Low level input	0V	-	0.6V
	Rp	Pull up/down resistor	10K ohm	-	100K ohm
P8	VDD_P8=1.8/2.5V				
	Rp	Pull up/down resistor	20K ohm	-	50K ohm

**Table 3: Pin description**

Pin name	Pin no.	Electrical description	Description	Comment
<b>Power supply</b>				
VBAT_BB	V45, V49, U47	PI $V_{MAX}=4.4V$ $V_{TYP}=3.8V$ $V_{MIN}=3.3V$	Input power supply for module's BB part	
VBAT_RF	Y49, AC47, AA47, W47, AD45, AB45, Y45	PI $V_{MAX}=4.4V$ $V_{TYP}=3.8V$ $V_{MIN}=3.3V$	Input power supply for module's RF part	
VDD_EXT	AL5	PO $V_{TYP}=1.8V$	Output power supply for external IO pull up circuits	
S2E_1P224	M45	PO $V_{TYP}=1.28V$	Output power supply for W80 only	
S3E_0P824	P49	PO $V_{TYP}=0.88V$	Output power supply for W80 only	
S4E_1P904	N47	PO $V_{TYP}=1.88V$	Output power supply for W80 only	
L10E_3P1	C41	PO $V_{TYP}=3.08V$	Output power supply for PM8150B USB PD-PHY and USB switch	
VIO_OUT	D42	PO $V_{TYP}=1.8V$	Output power supply for PM8150B IO circuit only	
GND	A7,B8,A11,B12,C15,A15,B16,C17,C19,D22,D24,D26,C27,A27,B		Ground	

28,D28,C31,C33,C35,C37,D40,A41,B42,J5,AD7,AJ1,AK3,AM3,AN1,AN5,AP3,AR1,AR5,AT3,AT7,AU1,AU5,AV3,AW1,R47,T49,U51,W51,AA51,AB49,AD49,AE47,AF45,AH45,AG47,AJ47,AL47,AN47,AR47,AU47,AV49,AW51,AV10,AV12,AV14,AV16,AV18,AV20,AV22,AV24,AV26,AV28,AV30,AV32,AV34,AV36,AV38,AV40,AV42,AW9,AW11,AW13,AW15,AW23,AW25,AW27,AW29,AW31,AW33,AW35,AW37,AW39,AW41,AW43,AY6,AY8,AY12,AY18,AY20,AY22,AY24,AY26,AY28,AY30,AY32,AY34,AY36,AY38,AY40,AY42,AY44,AY46,BA5,BA17,BA21,BA23,BA27,BA29,BA31,BA35,BA39,BA43,BA45,AM13,AM17,AM21,AM24,AM27,AM31,AM35,AM39,AH13,AH17,AH21,AH24,AH27,AH31,AH35,AH39,AE13,AE17,AE21,AE24,AE27,AE31,AE35,AE39,AA13,AA17,AA21,AA24,AA27,AA31,AA35,AA39,U13,U17,U21,U24,U27,U31,U35,U39,P13,P17,P21,P24,P27,P31,P35,P39,K13,K17,K21,K24,K27,K31,K35,K39,A1,B4,C7,A51,B48,C45,BA1,AY4,AW7,BA51,AY48,AW45

### System control

PWRKEY <sup>1</sup>	A45	DI	1.1V	Power on/off the module, active low	Pull up to 1.1V internally without PM8150B
PON_1	T45	DI	1.8V	Power on the module, active high	
RESIN_N	A43	DI	P3	Reset the module, active low	

### Status indicator

STATUS	AJ5	DO	P3	Indicate operation status of the module	
AP_STATUS	AH3	DI	P3	Indicate operation status of the AP	
NET_MODE	AE5	DO	P3	Indicate network registration mode of the module	
NET_STATUS	AE1	DO	P3	Indicate network activity status of the module	

### USB interface

USB_VBUS	C9	AI		USB VBUS detection	Not support charge
USB_HS_DP	B6	AIO		Differential USB bi-directional data plus	Required 90Ω differential impedance
USB_HS_DM	A5	AIO		Differential USB bi-directional data minus	Compliant with USB 2.0 standard specifications
USB_SS_TX_P	A13	AO		USB3.1 super-speed transmit data plus	Required 90Ω differential
USB_SS_TX_M	B14	AO		USB3.1 super-speed transmit data minus	Impedance Compliant with USB
USB_SS_	B10	AI		USB3.1 super-speed receive	3.1 standard

RX_P				data plus	specifications
USB_SS_RX_M	A9	AI		USB3.1 super-speed receive data minus	
USB_ID*	C11	DI	P3	USB ID	If unused, please keep open
OTG_EN*	D10	DO	P3	USB OTG power supply DC-DC enable signal	
USB_SS_SW	C13	DO	P3	USB Type-C switch control signal	

### (U)SIM interface

(U)SIM1_VDD	B51	PO		Power supply for (U)SIM1 card	
(U)SIM1_DATA	E51	DIO	P4	(U)SIM1 card data signal, which has been pulled up to (U)SIM1_VDD by a 20K resistor internally	
(U)SIM1_CLK	D49	DO	P4	(U)SIM1 clock signal	
(U)SIM1_RST	C51	DO	P4	(U)SIM1 reset signal	
(U)SIM1_DET	E47	DI	P3	(U)SIM1 card detect signal, which need pulled up to VDD_EXT by a 470K resistor externally	1.8/3.0V voltage domain, (U)SIM interface should be protected against ESD.
(U)SIM2_VDD	F49	PO		Power supply for (U)SIM2 card	If unused, please keep open
(U)SIM2_DATA	G47	DIO	P5	(U)SIM1 card data, which has been pulled up to (U)SIM1_VDD by a 20K resistor internally	
(U)SIM2_CLK	H49	DO	P5	(U)SIM2 clock signal	
(U)SIM2_RST	G51	DO	P5	(U)SIM2 reset signal	
(U)SIM2_DET	F45	DI	P3	(U)SIM1 card detect, which need pulled up to VDD_EXT by a 470KR resistor externally	

### SPI interface

SPI_CS_N	D18	DO	P3	SPI chip select	
SPI_CLK	D20	DO	P3	SPI clock	
SPI_MOSI	D14	DO	P3	Master output slaver input	
SPI_MISO	D16	DI	P3	Master input slaver output	

### UART1 interface

UART1_CTS	AA1	DO	P3	Clear to send	
UART1_RTS	AC1	DI	P3	Request to send	Default use for AT command
UART1_TXD	AB3	DO	P3	Transmit data	
UART1_RXD	AD3	DI	P3	Receive data	
UART1_DCD	W5	DO	P3	Carrier detect	If not need 7-wire UART, these signals
UART1_RI	AA5	DO	P3	Ring indicator	

UART1_DTR	AC5	DI	P3	Data terminal ready	can be used as GPIO
UART2 interface					
UART2_CTS	V3	DO	P3	Clear to send	
UART2_RTS	Y3	DI	P3	Request to send	
UART2_TXD	U1	DO	P3	Transmit data	
UART2_RXD	W1	DI	P3	Receive data	
BT UART interface					
BT_UART_CTS	R5	DO	P3	Clear to send	Default use for BT
BT_UART_RTS	U5	DI	P3	Request to send	
BT_UART_TXD	T7	DO	P3	Transmit data	
BT_UART_RXD	V7	DI	P3	Receive data	
Debug UART interface					
DBG_UART_RXD	L5	DI	P3	Receive data	Used for debug only
DBG_UART_TXD	N5	DO	P3	Transmit data	
I2C interface <sup>3</sup>					
I2C1_SCL	M7	OD	P3	I2C1 clock signal	I2C1 default use for codec Pull up to VDD_EXT externally
I2C1_SDA	P7	OD	P3	I2C1 data signal	
I2C2_SCL	AB7	OD	P3	I2C2 clock signal	I2C2 default use for sensor Pull up to VDD_EXT externally
I2C2_SDA	Y7	OD	P3	I2C2 data signal	
WLAN I2S interface					
WL_I2S_DOUT	K3	DO	P3	WLAN I2S data output	Default use for WLAN
WL_I2S_DIN	M3	DI	P3	WLAN I2S data input	
WL_I2S_CLK	J1	DO	P3	WLAN I2S bit clock	
WL_I2S_WS	G1	DO	P3	WLAN I2S word select	
I2S(PCM) interface					
I2S_DOUT/PCM_DOUT	N1	DO	P3	I2S/PCM data output	Default is I2S interface, can be configured as PCM interface by software, If unused, please keep open
I2S_DIN/PCM_DIN	R1	DI	P3	I2S/PCM data input	
I2S_CLK/PCM_CLK	P3	DO	P3	I2S/PCM clock output	
I2S_WS/PCM_SYNC	T3	DIO	P3	I2S word select/ PCM synchronous signal	
I2S_MCLK	L1	DO	P3	I2S master clock output	
ADC interface					
ADC0	AH7	AI		Analog to digital converter input0	

ADC1	AF7	AI		Analog to digital converter input1	
<b>RGMIi interface<sup>4</sup></b>					
RGMIi_MD_IO	D30	DIO	P8	RGMIi management data	Required 50Ω impedance
RGMIi_MD_CLK	D34	DO	P8	RGMIi management data clock	
RGMIi_RX_CTL	A35	DI	P8	RGMIi receive control	
RGMIi_RX_CLK	B36	DI	P8	RGMIi receive clock	
RGMIi_RX_0	B40	DI	P8	RGMIi receive data bit 0	
RGMIi_RX_1	A37	DI	P8	RGMIi receive data bit 1	
RGMIi_RX_2	B38	DI	P8	RGMIi receive data bit 2	
RGMIi_RX_3	A39	DI	P8	RGMIi receive data bit 3	
RGMIi_TX_CTL	A33	DO	P8	RGMIi transmit control	
RGMIi_TX_CLK	B34	DO	P8	RGMIi transmit clock	
RGMIi_TX_0	A31	DO	P8	RGMIi transmit data bit 0	
RGMIi_TX_1	B30	DO	P8	RGMIi transmit data bit 1	
RGMIi_TX_2	A29	DO	P8	RGMIi transmit data bit 2	
RGMIi_TX_3	B32	DO	P8	RGMIi transmit data bit 3	
RGMIi_INT_N	C39	DI	P3	Interrupt input from RGMIi PHY	
RGMIi_RST_N	C29	DO	P3	Reset output to RGMIi PHY	
RGMIi_PWR_EN	D36	DO	P3	Used to enable external LDO to supply 2.5V power to RGMIi_PWR_IN	
RGMIi_PWR_IN	D32	PI	1.8/2.5V	Power supply input for internal RGMIi circuit	Default connect to VDD_EXT externally
RGMIi_3P3_EN	D38	DO	P3	Used to enable external DC-DC/LDO to supply 3.3V power to RGMIi PHY	
<b>PCle interface<sup>5</sup></b>					
PCle_REFCLK_P	B22	AIO		PCle reference clock plus	Required 90 Ω differential impedance
PCle_REFCLK_M	A21	AIO		PCle reference clock minus	
PCle_TX0_M	B18	AO		PCle transmit0 minus	
PCle_TX0_P	A17	AO		PCle transmit0 plus	
PCle_TX1_M*	B20	AO		PCle transmit1 minus	
PCle_TX1_P*	A19	AO		PCle transmit1 plus	
PCle_RX0_M	A25	AI		PCle receive0 minus	
PCle_RX0_P	B26	AI		PCle receive0 plus	
PCle_RX1_M*	A23	AI		PCle receive1 minus	

PCle_RX1_P*	B24	AI		PCle receive1 plus	
PCle_CLKREQ	C21	DI	P3	PCle clock request	CLKREQ and WAKE need pull up to VDD_EXT externally, Default as RC mode
PCle_WAKE	C25	DI	P3	PCle wake-up	
PCle_RST	C23	DO	P3	PCle reset	
W80 interface					
WL_SW_CTRL	K49	DO	P3	W80 switch control	
SDX_TO_WL_CTI	M49	DO	P3	W80 GPIO	
WL_TO_SDX_CTI	L47	DI	P3	W80 GPIO	
BT_EN	N51	DO	P3	W80 BT enable	
SLEEP_CLK	J51	DO		Sleep clock output for W80 only	
WL_EN	K45	DO	P3	WLAN enable	
WL_LAA_RX	J47	DI	P3	WLAN XFEM control for LAA receiver	W80 RF coexistence signals
WL_PA_MUTING	H45	DO	P3	WLAN XFEM control for PA mute	
WL_LAA_AS_EN	L51	DO	P3	WLAN LAA AS enable	
WL_LAA_TX_EN	R51	DO	P3	WLAN XFEM control for LAA enable	
COEX_UART_TXD	BA7	DO	P3	LTE&WLAN coexistence data transmit	
COEX_UART_RXD	BA9	DI	P3	LTE&WLAN coexistence data receive	
WL_TX_EN	AY14	DI	P3	WLAN XFEM control for WLAN TX enable	
WL_SW_CTRL	K49	DO	P3	W80 switch control	
SDIO interface					
SDIO_VDD	F7	PI	1.8/3.0V	Power input for internal SDIO circuit	
SDIO_DATA0	B1	DIO	P2	SDC data bit 0 or eMMC* data bit 0	Required 50Ω impedance
SDIO_DATA1	C1	DIO	P2	SDC data bit 1 or eMMC data bit 1	
SDIO_DATA2	D3	DIO	P2	SDC data bit 2 or eMMC data bit 2	
SDIO_DATA3	F3	DIO	P2	SDC data bit 3 or eMMC data bit 3	
SDIO_CMD	G5	DIO	P2	SDC command output	
SDIO_CLK	E5	DO	P2	SDC clock output	If used as eMMC
SDIO_VDD_EN	H7	DO	P3	Enable the SD card power or	



				eMMC data bit 4	data signals, required 50Ω impedance
SDIO_DET	E1	DI	P3	SD card insertion detect or eMMC data bit 5	
GPIO100	H3	DIO	P3	eMMC data bit 6	
GPIO101	K7	DIO	P3	eMMC data bit 7	
RESOUT_N*	AW17	DO	P3	eMMC RST_N	
PM8150B interface					
CHG_SYS_OK	C43	DI		When charger input is inserted PM8150B output signal to PMU	Used for PM8150B only
FAULT_N	B44	DIO		Used to send/receive the fault condition across all PMICs in the chipset	
SPMI_CLK	A47	DO		SPMI communication bus clock signal	Required 50Ω impedance
SPMI_DATA	B46	DIO		SPMI communication bus data signal	
Other interface					
EMAC_OUT*	AY10	DO	P3	1PPS time sync output	
USB_BOOT	D12	DI	P3	Module will be forced into USB boot mode by connect this pin to VDD_EXT externally	
W_DISABLE	AG1	DI	P3	Flight mode control input active low	
SLEEP_IN	AG5	DI	P3	Sleep mode control input	
WAKEUP_OUT	AF3	DO	P3	Module wake up the external AP	
CDC_RST_N	AK7	DO	P3	Module reset the external CODEC active low	
CDC_INT_N	AM7	DI	P3	External CODEC interrupt input active low	
Antenna control interface <sup>6</sup>					
RFFE0_CLK	BA11	DO	P3	Antenna tuner MIPI CLK	
RFFE0_DATA	BA13	DIO	P3	Antenna tuner MIPI DATA	
ANT_CTRL0	BA15	DO	P3	Antenna tuner control0	
ANT_CTRL1	AY16	DO	P3	Antenna tuner control1	
ANT interface					
ANT0	AL1	AIO		LTE low/middle/high BAND signal send and receive; n41 signal send and receive; n79 signal diversity receive	617MHz~960MHz 1710MHz~2690MHz 4400MHz~5000MHz
ANT1	BA25	AI		LTE middle/high band signal diversity receive; n41&n77 signal diversity	1710MHz~2690MHz 3300MHz~4200MHz



				receive	
ANT2	BA41	AIO		LTE low/middle/high band signal diversity receive; N79 signal send and receive	617MHz~960MHz 1710MHz~2690MHz 4400MHz~5000MHz
ANT3	AY51	AIO		LTE middle/high BAND signal diversity receive; n41 signal diversity receive; n77 signal send and receive	1710MHz~2690MHz 3300MHz~4200MHz
ANT4	BA33	AIO		n41 signal send and receive; n77 signal diversity receive	2496MHz~2690MHz 3300MHz~4200MHz
ANT5	BA19	AIO		n77 signal send and receive	3300MHz~4200MHz
ANT6	AY1	AI		n79 signal diversity receive; GNSS signal receive ;	1166MHz~1229MHz 1565MHz~1610MHz 4400MHz~5000MHz
ANT7	BA47	AIO		n79 signal send and receive	4400MHz~5000MHz
<b>RFU interface</b>					
RFU	AP7,AW19,AW21,AT45,AP45,AM45,AK45,AG51,AU51,AR51,AN51,AJ51,AL51,AE51,AC51,BA37,AT49,AP49,AM49,AK49,AH49,AF49,P45,D9		Reserved for future use		

#### NOTE

1. PWRKEY will be pulled up to 1.8V internally if used PM8150B.
2. "\*" means under development.
3. The I2C signals need pull up to VDD\_EXT by 2.2K resistors out of the module.
4. If not use RGMII function, the RGMII\_PWR\_IN pin should connect to VDD\_EXT out of the module.
5. If not use SDIO function, the SDIO\_VDD pin should connect to VDD\_EXT out of the module.
6. Please confirm with SIMCom for the detail design about Antenna control interface.
7. Only used to W80 and PM8150B pins don't use as other circuits.
8. Unused and RFU pins should keep open.
9. Recommend ESD protect components out of the module for used interfaces.
10. The GPIO MAX voltage is 2.1V, if exceeded, may cause permanent damage to the module.
11. All GND pins should be connected to the customer's main PCB.

## 2.3 GPIO Alternate function

**Table 4: GPIO Alternate Function List**

PIN Name	PIN No.	GPIO	Default function	Alternate function 1	interrupt function
UART2_TXD	U1	GPIO2	UART2_TXD	SPI_MOSI	⌚
UART2_RXD	W1	GPIO5	UART2_RXD	SPI_MISO	⌚
UART2_CTS	V3	GPIO6	UART2_CTS	SPI_CS_N	⌚
UART2_RTS	Y3	GPIO7	UART2_RTS	SPI_CLK	
I2S_WS	T3	GPIO12	I2S_WS	PCM_SYNC	⌚
I2S_DIN	R1	GPIO13	I2S_DIN	PCM_DIN	⌚
I2S_DOUT	N1	GPIO14	I2S_DOUT	PCM_DOUT	⌚
I2S_CLK	P3	GPIO15	I2S_SCK	PCM_CLK	⌚
WL_I2S_WS	G1	GPIO16	WL_I2S_WS	SPI_MOS	⌚
WL_I2S_DIN	M3	GPIO17	WL_I2S_DIN	SPI_MISO	⌚
WL_I2S_DOUT	K3	GPIO18	WL_I2S_DOUT	SPI_CS_N	⌚
WL_I2S_CLK	J1	GPIO19	WL_I2S_SCK	SPI_CLK	⌚
UART1_TXD	AB3	GPIO20	UART1_TX	I2S_WS	
UART1_RXD	AD3	GPIO21	UART1_RX	I2S_DIN	⌚
UART1_CTS	AA1	GPIO22	UART1_CTS	I2S_DOUT	⌚
UART1_RTS	AC1	GPIO23	UART1_RTS	I2S_SCK	⌚
BT_UART_TXD	T7	GPIO63	BT_UART_TX		
BT_UART_RXD	V7	GPIO64	BT_UART_RX		⌚
BT_UART_CTS	R5	GPIO65	BT_UART_CTS	I2C_SDA	⌚
BT_UART_RTS	U5	GPIO66	BT_UART_RTS	I2C_SCL	
SPI_MOSI	D14	GPIO80	SPI_MOSI		
SPI_MISO	D16	GPIO81	SPI_MISO		
SPI_CS_N	D18	GPIO82	SPI_CS	I2C_SDA	
SPI_CLK	D20	GPIO83	SPI_CLK	I2C_SCL	⌚
CDC_RST_N	AK7	GPIO92	CDC_RST_N		
CDC_INT_N	AM7	GPIO96	CDC_INT_N		⌚

## 2.4 Mechanical Information

The following figure shows the mechanical dimensions of SIM8200G.

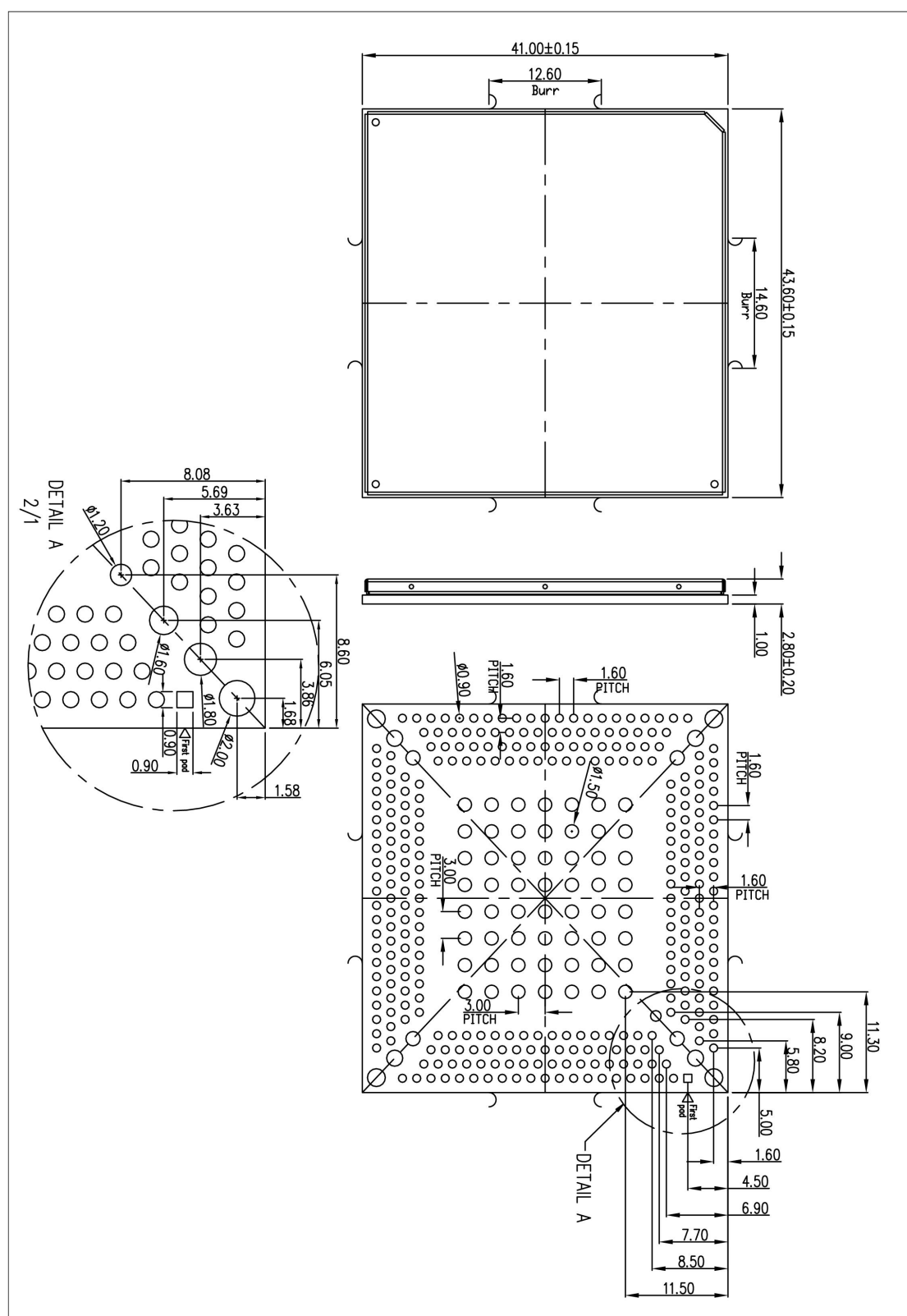


Figure 3: Dimensions of SIM8200G (unit: mm)

## 2.5 Recommended PCB Footprint

The following figure shows the PCB footprint of SIM8200G.

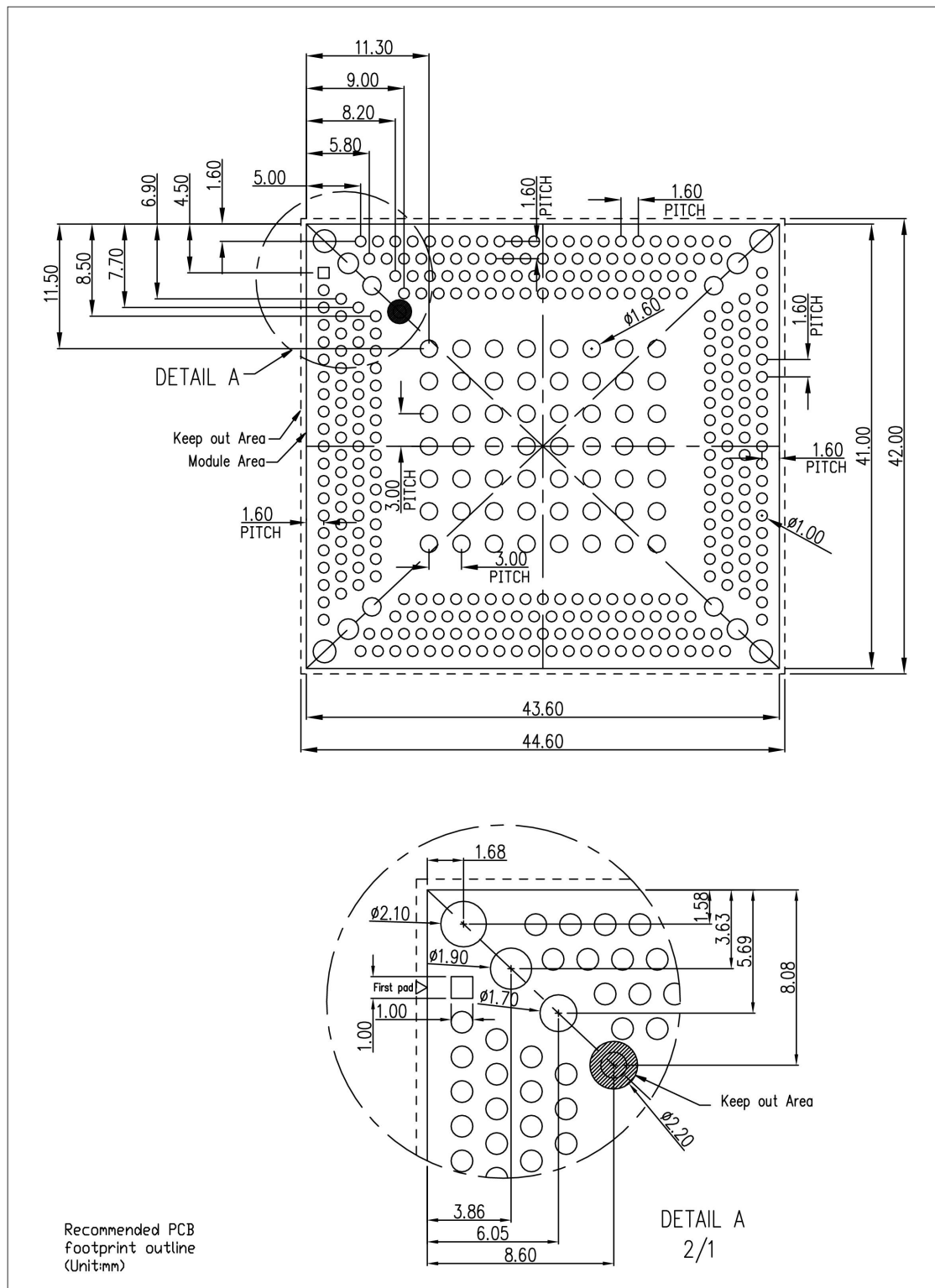


Figure 4: Recommended PCB footprint

## 2.6 Recommended SMT Stencil

The following figure shows the SMT stencil of SIM8200G.

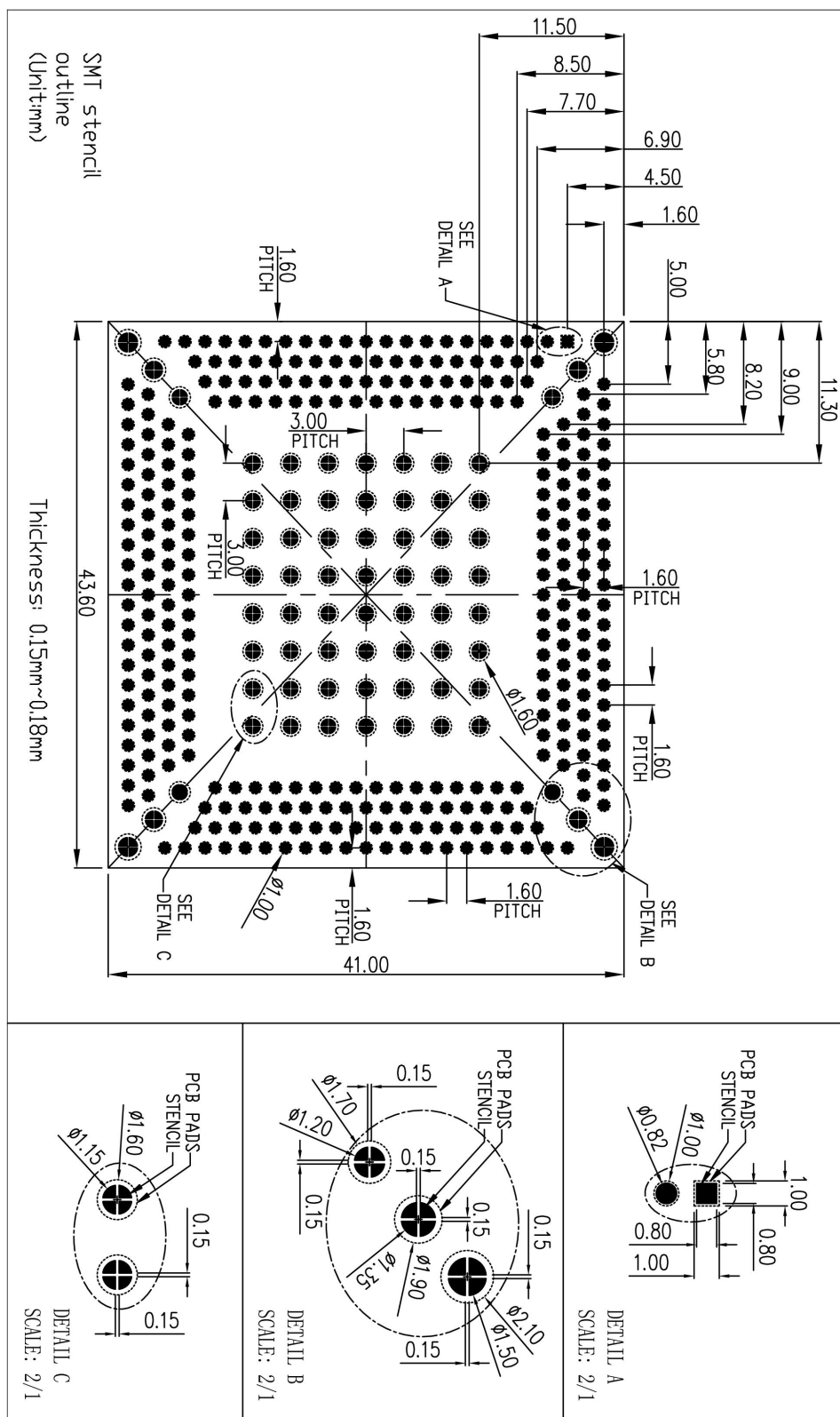


Figure 5: Recommended SMT stencil

## 2.7 Recommended SMT Reflow Profile

The following figure shows the SMT reflow profile of SIM8200G.

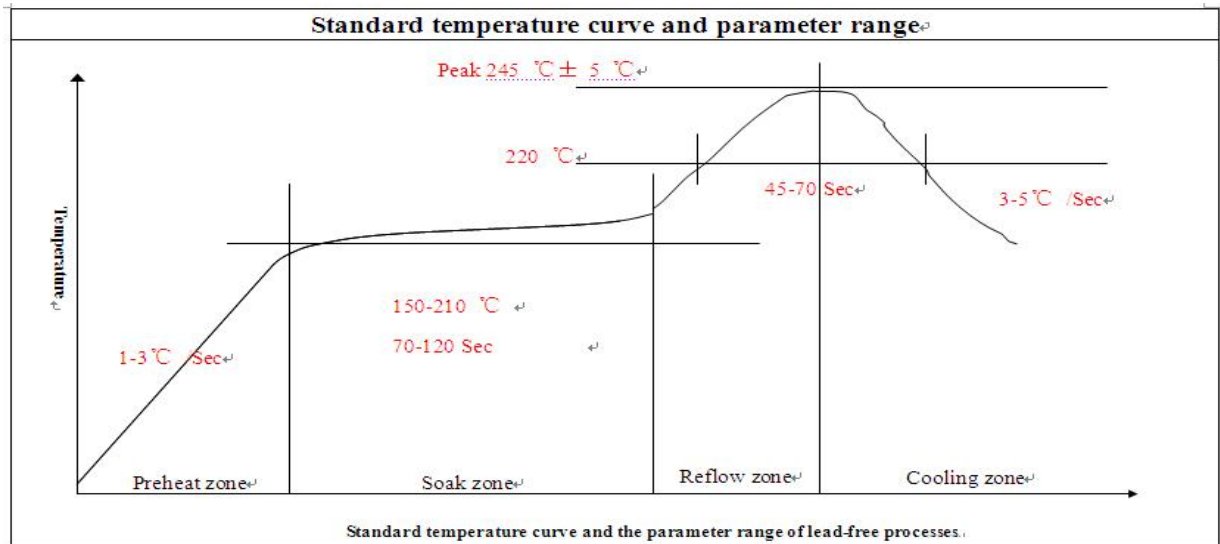


Figure 6: Recommended SMT reflow profile

### NOTE

Refer to “Module secondary-SMT-UGD” for more information about the module shipping and manufacturing.